Abstract of the Disclosure

A synchronous flash memory includes an array of non-volatile memory cells. The memory array is arranged in rows and columns, and can be further arranged in addressable blocks. Data communication connections are used for bi-directional data communication with an external device, such as a processor or other memory controller. A data buffer can be coupled to the data communication connections to manage the bi-directional data communication. This buffer can be a pipelined input/output buffer circuit. Finally, a write latch is coupled between the data buffer and the memory array to latch data provided on the data communication connections. One method of operating a synchronous memory device comprises receiving write data on data connections, latching the write data in a write latch, and releasing the data connections after the write data is latched. A read operation can be performed on the synchronous memory device while the write data is transferred from the write latch to memory cells. Further, the memory device does not require any clock latency during a write operation.